REMARKS

Claims 13, 14, 16, 17, 41 and 42 are pending in this application. Claim 15 has been canceled. Claims 13, 14 and 41 have been amended.

Claims 13, 16, 17, 41 and 42 stand rejected under 35 U.S.C. §102 as being anticipated by Luan et al., *Ultra Thin High Quality Ta2O5 Gate Dielectric Prepared By In-Situ Rapid Thermal Processing*, IEEE 1998, pp. 609-612 ("Luan"). This rejection is respectfully traversed.

The claimed invention relates to a method of fabricating a semiconductor device according to which a dielectric film is subjected to wet oxidation in a rapid thermal process chamber. As such, amended independent claim 13 recites a method of fabricating a semiconductor device by "depositing a dielectric film over an active region of a semiconductor substrate to form part of a gate of a transistor" and "subjecting the dielectric film to a wet oxidation with steam provided by heating a mixture of hydrogen and oxygen gases in a rapid thermal process chamber at a temperature greater than about 450 °C." Amended independent claim 41 recites a method of fabricating a semiconductor device by "depositing a dielectric film with a thickness greater than about 40 Angstroms over a semiconductor substrate" and "subjecting the dielectric film to a wet oxidation in a rapid thermal process chamber at a temperature greater than about 450 °C." Independent claim 42 also recites "depositing a dielectric film over a semiconductor substrate to form one of a gate and a capacitor dielectric" and "subjecting the dielectric film to a wet oxidation in a rapid thermal process chamber at a temperature greater than about 450 °C."

Luan relates to "ultra thin CVD Ta_2O_5 gate dielectrics . . . fabricated by *in-situ* RTP processing." (Abstract). According to Luan, a Ta_2O_5 gate stack is formed by growing an NO bottom passivation layer and then depositing a Ta_2O_5 film "using Ta precursor . . . and O_2 at 420°C for 20 sec." (Experiment, p. 609). Luan teaches that "[P]ost deposition annealing is performed in O_2 or H_2/O_2 ambient at 600°C to improve film quality and reduce leakage current." (Experiment, p. 609).

Luan does not teach or suggest the limitations of the claimed invention. Luan does not teach or suggest the formation of a semiconductor device by "depositing a dielectric film over an active region of a semiconductor substrate to form *part of a gate of a transistor*" and "subjecting the dielectric film to a *wet oxidation with steam* provided by heating a mixture of hydrogen and oxygen gases in a rapid thermal process chamber," as amended independent claim 13 recites (emphasis added). Luan teaches a "Ta_2O_5 gate stack" of a "LOCOS isolated *MOS capacitor*," and not a "dielectric film over an active region of a semiconductor substrate to form *part of a gate of a transistor*," as recited in amended independent claim 13 (emphasis added). In addition, Luan teaches "dry O_2 anneal or H_2/O_2 anneal" (Figure 1), and not "a *wet oxidation* with steam provided by heating a mixture of hydrogen and oxygen gases in a rapid thermal process chamber," as amended independent claim 13 recites (emphasis added).

Luan also fails to teach or suggest the limitations of independent claims 41 and 42. Luan does not teach or suggest "depositing a dielectric film with a thickness greater than about 40 Angstroms over a semiconductor substrate" (claim 41) or "depositing a dielectric film over a semiconductor substrate to form one of a gate and a capacitor dielectric" (claim 42). Luan specifically emphasizes that the ultra thin CVD Ta_2O_5 gate dielectrics have a thickness less than 15 Angstroms (Introduction, p. 609) and not "greater than about 40 Angstroms," as amended independent claim 41 recites. Further, Luan teaches a Ta_2O_5 gate stack of a "LOCOS isolated MOS capacitor" and not "a dielectric film over a semiconductor substrate to form one of a gate and a capacitor dielectric," as recited in independent claim 42. For at least these reasons, the limitations of claims 13, 16, 17, 41 and 42 are not described in Luan, and the claimed invention is not anticipated by Luan.

Claim 14 stands rejected under 35 U.S.C. §103 as being unpatentable over Tseng et al. (US Patent No. 6,063,698) ("Tseng"). This rejection is respectfully requested.

Amended claim 14 depends on amended independent claim 13 and recites that "the wet oxidation process is performed at a temperature in the range of about 750 °C to about 950 °C and for a duration of about 20 seconds to about 60 seconds."

Tseng relates to a method of forming a high dielectric constant gate oxide 14b without bulk traps and interface traps. (Abstract). Tseng teaches that dielectric layer 14a and gate electrode 20 are exposed to a "wet oxidation ambient (23) which is supplied with both O_2 gas and H_2 gas." (Col. 5, lines 54-58; Figure 3). Tseng notes that "[T]he typical time of exposure for the environment 23 is preferably 15 minutes." (Col. 5, lines 62-53). Tseng further specifies that "the time of exposure to the environment 23 may be changed to a length of time between 10 minutes and 1 hour." (Col. 5, lines 63-65).

The subject matter of claim 14 would not have been obvious over Tseng. Indeed, the Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 U.S.P.Q.2d 1626, 1630 (Fed. Cir. 1996).

In the present case, Tseng fails to teach or suggest all limitations of amended dependent claim 14. Tseng fails to teach or suggest wet oxidation of a dielectric film "at a temperature in the range of about 750 °C to about 950 °C and for a duration of about 20 seconds to about 60 seconds," as amended claim 14 recites. As noted above, Tseng teaches that "the time of exposure to the environment 23 may be changed to a length of time between 10 minutes and 1 hour" (col. 5, lines 63-65), and not to "a duration of about 20 seconds to about 60 seconds," as recited in amended claim 14. For at least these

reasons, the subject matter of claim 14 would not have been obvious over Tseng, and withdrawal of the rejection of this claim is respectfully requested.

A marked-up version of the changes made to the specification and claims by the current amendment is attached. The attached page is captioned "**Version with markings to show changes made.**"

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

13. (twice amended) A method of fabricating a semiconductor device, the method comprising:

depositing a dielectric film over an active region of a semiconductor substrate to form part of a gate of a transistor; and

subjecting the dielectric film to a wet oxidation with steam provided by heating a mixture of hydrogen and oxygen gases in a rapid thermal process chamber at a temperature greater than about 450 °C.

14. (amended) The method of claim 13 wherein the wet oxidation process is performed at a temperature in the range of about 750 °C to about 950 °C and for a duration of about 20 seconds to about 60 seconds.

41. (amended) A method of fabricating a semiconductor device, the method comprising:

depositing a dielectric film with a thickness greater than about 40 Angstroms over a semiconductor substrate; and

subjecting the dielectric film to a wet oxidation in a rapid thermal process chamber at a temperature greater than about 450 °C.

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